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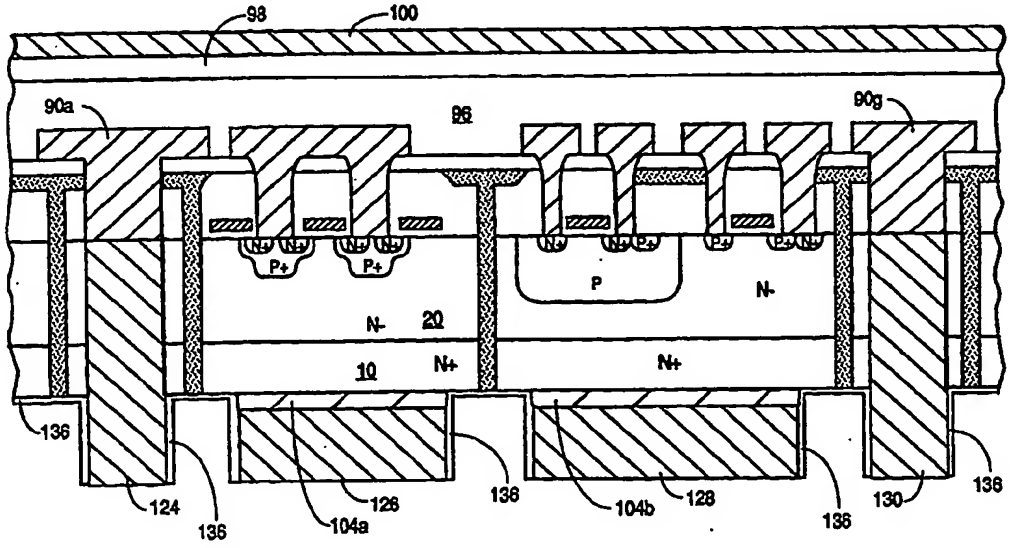

(57) Abstract

An integrated circuit chip has full trench dielectric isolation of each portion of the chip. A heat sink cap (100) is attached to a diamond passivation layer (96) on the substrate front side surface. The passivation layer is a CVD diamond film which provides both electrical insulation and thermal conductivity. In a flip chip version, frontside electrical contacts (174a, 174b) extend through the frontside passivation layer to the heat sink cap. In a surface mount version, vias are etched through the substrate, with surface mount posts (90a, 90g) formed on the vias, to contact the frontside electrical contacts and provide all electrical contacts on the substrate backside surface. The wafer is then scribed into die in both versions without need for further packaging.

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SURFACE MOUNT AND FLIP CHIP TECHNOLOGY

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to integrated circuit electrical isolation, and more specifically to integrated circuit total isolation using both surface mount and flip chip fabrication technologies with a diamond film passivation layer.

Description of the Prior Art

Dielectric isolation for integrated circuits is well known. A trench or groove is formed in the semiconductor chip substrate and is lined or filled with an insulative material, to electrically isolate various portions of the chip. For instance, a particular portion of the chip such as power (high voltage) transistors is surrounded by an insulated trench, thereby electrically isolating the power transistors from logic type (low voltage) transistors.

This prior art trench isolation has the significant disadvantage that the bottom of each trench is an area of substantial mechanical stress in the silicon substrate, thereby being detrimental to chip functionality. Such trenches thus reduce yield (increase cost). This deficiency is sometimes overcome by using "round hole" techniques to form the bottom of

each trench (providing a U-shaped rather than a rectangular cross-section) which however, also tends to increase cost.

Another method for achieving isolation uses two wafers, with an oxide layer formed on a surface of one wafer which is then bonded to the second wafer; the oxide layer provides the isolation. After bonding the two wafers, the backside of one of the wafers is polished away down to the oxide layer to isolate a portion of the remaining substrate. However, this is very expensive because there can be no defects in the bond between the two wafers. Defects are often induced by particles in the bond between the two wafers, causing low production yield and hence high cost. Also, oxidation induced stacking faults (OISF) due to processing temperature cycles are undesirably more pronounced in such a bond than in bulk silicon.

Therefore, the prior art is deficient in not providing practical and inexpensive dielectric isolation, especially for use with power transistors but also for other types of integrated circuits.

SUMMARY OF THE INVENTION

An integrated circuit structure and a fabrication method use trench dielectric isolation. This trench dielectric isolation is part of a chip fabrication process which allows the packaging for each chip to be formed on the wafer, thereby eliminating the prior art separate step of packaging a semiconductor die after the wafer is scribed into multiple die. Therefore the disclosed process is the equivalent of assembly or packaging the integrated circuit die at "waferscale", since each die is already packaged before the wafer is scribed.

In accordance with the invention, transistors (or other semiconductor devices) are conventionally

fabricated on a semiconductor substrate. Some of these devices may be power transistors (operating at high voltage) and others may be lower voltage logic-type transistors formed in another portion of the substrate. In one embodiment, the devices are field effect transistors having gate electrodes formed in an insulated layer overlying the principal surface of the semiconductor substrate. Alternatively, the transistors are IGBT's (insulated gate bipolar transistors), or bipolar transistors, or other semiconductor devices. The fabrication process technology may be a CMOS, NMOS, PMOS, DMOS, BiCMOS, or bipolar technology, for example. Then an interconnect pattern is conventionally formed overlying and interconnecting the gate electrodes (or other transistor elements), and for contacting the semiconductor regions (e.g. source and drain) formed in the substrate.

A plurality of insulated trenches are then formed penetrating the principal surface of the substrate into the depth thereof, and surrounding (in a top view) various portions of the substrate. The trenches are conventionally insulated by filling or lining them with an insulative material followed by a planarization. This step may be prior to metallization. Then a portion of the backside of the substrate is removed by conventional machining or chemical processes, exposing the bottom portion of each of the trenches, and thereby achieving full (total) electrical isolation of the various substrate portions surrounded by each trench.

Prior to the step of removing the backside portion of the substrate, the frontside surface is bonded to a heat sink cap or plate (made for instance of silicon) using epoxy or similar bonding materials. This heat sink cap also provides the needed mechanical support for the substrate, which is otherwise quite thin

following the substrate removal step.

Electrical contact is achieved in two different embodiments. In a surface mount embodiment, vias penetrate from the backside surface of the substrate to its principal (frontside) surface, allowing electrically conductive material formed in the vias to contact an interconnect structure already formed on the substrate frontside surface. Extensions of the vias on the substrate backside define posts for surface mount electrical contacts. Other similar posts formed on the backside surface of the substrate make contact to the bulk substrate. The heat sink cap attached to the frontside substrate surface has a mechanical and heat dissipation function, with no electrical connections provided thereby.

In a flip chip type embodiment, the heat sink cap also carries on it an electrical interconnect, making electrical contact to the conventional interconnect on the substrate frontside surface. This heat sink cap may be attached to a conventional flip chip backplate. In this embodiment the electrical contacts formed on the substrate backside surface are the conventional drain or collector contacts for e.g. power integrated circuits.

In both embodiments, the individual integrated circuits are packaged while still being part of a single wafer, by the application of the heat sink cap which is attached (by epoxy or other adhesive) to the wafer frontside surface. This cap replaces the conventional plastic or ceramic packaging which in the prior art is applied only after the wafer is scribed into individual die. In the present case the full trench isolation between the die allows the die to be scribed adjacent to the isolation trenches, together with attached front end mechanical support plate (cap), so no further packaging is needed.

Typically, the thickness of the substrate after the substrate removal step is less than about 50 micrometers. This very thin substrate is free of heat induced mechanical stresses, due to its mechanical flexibility. Advantageously, integrated circuit chips in accordance with the invention are inexpensively fabricated using essentially conventional steps which provide a high yield, thus reducing cost.

The dielectric isolation trenches may conventionally be lined, for instance with silicon dioxide (formed from the silicon trench walls), or may be completely filled with silicon dioxide, or may be lined with silicon dioxide and then filled with another material such as CVD (chemical vapor deposition) nitride, polysilicon or oxide. In another embodiment, the trenches are filled with conventional spun on glass. Other insulating materials may be used for the trench dielectric.

The heat sink cap (plate) is typically silicon, silicon carbide, silicon nitride, aluminum nitride, molybdenum, or other material which provides sufficient heat transfer and is conveniently fabricated. The removal of the backside of the substrate advantageously eliminates mechanical stresses normally present at the bottom of a trench formed in silicon. Thus the principal problem with prior art trench isolation is overcome, resulting in a thin, flexible substrate.

Also, the prior art requirement for a semiconductor buried layer in the substrate is eliminated, due to the very thin substrate and formation of a layer of conductive material on selective areas of the substrate backside surface. Thus the processing problems associated in the prior art with establishing an effective buried layer are avoided, and the parasitic bipolar transistor effects typically present in prior art integrated circuits

(especially for power integrated circuits) are eliminated by a backside contact which is a metal plate or metallization layer rather than a buried semiconductor layer.

The metallized drain (or collector) contact on the backside surface, which is in relatively close proximity to the active transistors (due to the thinness of the substrate), increases current carrying capability over that of the prior art chips which require either the buried layer or current being transmitted through the relatively thick bulk of the semiconductor substrate. Thus advantageously the actual thickness of the final substrate itself is the minimum necessary to support (mechanically and electrically) the active transistor regions. This thickness may be as little as 10 microns, in contrast to prior art integrated circuits typically having a 400 micron die thickness needed for mechanical support for the integrated circuit.

Additionally, the step of removing the backside portion of the substrate after trench formation means that the initial trench depth need not be precisely determined. In the prior art, formation of trenches of precise depth is a significant processing limitation. In the present case, since the bottom portion of each trench is removed, exact trench depth is not critical.

Also, the fabrication process in accordance with the invention advantageously allows for an isolated backside contact structure which is not a single contact but a plurality of individual backside contacts, each contact associated with a particular portion of the die. This allows for instance a first backside contact to a power transistor portion of the integrated circuit, and a second backside contact associated with a low voltage transistor portion of the integrated circuit. Thus the backside contacts are

selectable for a particular portion of the integrated circuit, and various portions of the chip need not share a common collector or common drain.

In another embodiment, the passivation layer which serves as an isolation layer and an attachment layer to bond the IC wafer (substrate) to the heat sink cap or plate is a CVD (Chemical Vapor Deposition) diamond film. Such material advantageously has high thermal conductivity and high electric resistivity. The diamond film is deposited on top of the substrate after the final front side surface metal patterning. A thermally conductive adhesive (such as silver epoxy) is applied to the exposed surface of the deposited diamond film to attach the substrate to the plate. This use of diamond film is compatible both with the surface mount and flip chip embodiments described above. In accordance with the invention the diamond layer may be patterned so that particular portions of the metal contact or bonding pads are connected to and through the support plate to external leads from the front side of the wafer, in the flip chip embodiment.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1 to 12 illustrate exemplary fabrication steps of the surface mount embodiment of the invention.

Figs. 13 to 17 illustrate exemplary fabrication steps of the flip chip type embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

Surface Mount Embodiment

Figs. 1 to 12 illustrate steps to fabricate a surface mount integrated circuit chip in accordance with the invention. It is understood that these are conventionally drawn cross sections of an integrated

circuit showing only a small portion of the circuit, i.e. a small portion of a wafer. No topside views are provided, since the top side geometry of the integrated circuit is conventional, as will be understood by one of ordinary skill in the art from the following description. Also, this is only an illustration of the surface mount approach, which is not limited to semiconductor devices of the type shown.

Fig. 1 shows initial steps in fabrication of this embodiment. Fig. 1 is conventional both in structure and fabrication as typically used for integrated circuits which include both power transistors and low voltage transistors on one chip. See U.S. Patent Application No. 07/948,276, filed 9/21/92, Hamza Yilmaz et al., entitled "BiCDMOS Process Technology and Structure", incorporated by reference, for an example of such a fabrication process. Shown in Fig. 1 is silicon (or other material) substrate 10 which is conventionally N+ doped, having formed on an upper portion thereof in one embodiment an epitaxial (silicon) layer 20 which is conventionally N- doped. The epitaxial layer is an option but is not a necessary part of the invention; the active portions of the transistors may be formed in the substrate. (It is to be understood that materials, dimensions, transistor structure, conductivity types, and other elements disclosed herein are illustrative only and not limiting.)

Substrate 10 is approximately 500 micrometers thick, and silicon layer 20 is 1 to 50 micrometers thick. Conventionally formed (in this illustrative embodiment) in silicon layer 20 are two "deep body" conventionally doped P+ regions 22 and 24. Formed respectively in body regions 22 and 24 are N+ source regions 26, 28, 30 and 32 each of which is conventionally doped. It is to be appreciated that in

this embodiment P+ body regions 22 and 24 and the associated other doped regions are a part of a power portion of the integrated circuit, i.e. power transistors.

Formed adjacent to regions 22 and 24 is P tub 38 which is conventionally doped. Formed in P tub 38 are N+ doped regions 40 and 42. Also formed in silicon layer 20 are P+ regions 46 and 48 which are similar in their doping level and structure to region 44, and N+ region 50 which is similar to regions 40 and 42. Formed immediately overlying the upper surface of silicon layer 20 is a conventional gate oxide layer 60 of e.g. silicon dioxide.

Formed conventionally overlying oxide gate layer 60 is a doped polysilicon gate electrode layer 54 including (as a result of a masking step) portions 54a, 54b, 54c and 54d and 54e which in this embodiment form the gate electrodes of various transistors.

Overlying gate electrode layer 54 is a second overlying (upper) insulative layer 62 formed of silicon dioxide and also covering the respective side edges of the gate electrodes 54a, ..., 54e.

Overlying upper oxide layer 62 is a BPSG layer 64 (borophosphorsilicate glass) formed to a thickness of 0.5 to 1.5 micrometers and then conventionally reflowed to completely cover gate electrodes 54a, ..., 54e.

Fig. 2 shows subsequent processing with a conventional masking layer 70 formed overlying BPSG layer 64. Masking layer 70 is conventionally patterned and the underlying structure etched, with the etchant penetrating through silicon layer 20 and into substrate 10 to define trenches 72a, 72b, 72c, 72d, and 72e. These trenches are 0.5 to 5 micrometers in width and 5 to 50 micrometers in depth. (The depth is relatively arbitrary for reasons discussed later and the width dimension is also not critical.) The trench etch is a

conventional anisotropic process. It is to be understood that trenches 72a, ..., 72e as shown here in cross-section, would in a topside view interconnect so as to surround various portions of the integrated circuit, i.e. so as to surround the power transistor portion 22, 24 thereby separating this portion from the portion including P tub 38.

Then (not shown) the remaining portions of masking layer 70 are conventionally stripped off.

Next in Fig. 3, a glass layer 76 is formed conventionally such as by being spun on in each of trenches 72a, ..., 72e thereby filling each of these trenches, and also overlying the upper surface of BPSG layer 64, to a thickness of 1 to 2 micrometers. Alternatives to SOG for layer 76 are CVD formed materials or plasma enhanced CVD formed materials. After formation of spun on glass layer 76, this material is cured. Spun on glass 76 here is the trench dielectric insulating material. In other embodiments, the trenches e.g. are lined with a layer of grown silicon dioxide and then filled with another material such as CVD oxide, or nitride, or polysilicon. (These are conventional processes for forming dielectric layers.)

Next in Fig. 4, first an etch back (planarization) step using for instance CMP of the spun on glass layer 76 effectively removes those parts of layer 76 overlying the gate electrodes 54a, ..., 54e. An alternative to CMP is to apply a layer of photoresist then etch back using a dry etch.

Following the etch back step, an LTO (low temperature oxide) layer 80 is deposited over the upper surface of the structure to a thickness of 0.5 to 2.0 micrometers. Following the LTO layer 80 deposition, an electrical contact mask layer (not shown) is applied overlying LTO layer 80. The contact mask layer is then

conventionally patterned and the underlying layers etched, with the etch extending through LTO layer 80, through the remaining portions of spun on glass layer 76, and down to the principal surface of the silicon layer 20, thus exposing portions of the principal surface of the silicon layer 20 and defining contact openings 84a, ..., 84g.

Next in Fig. 5, a layer of conductive material 90 (such as aluminum) is conventionally deposited over the surface of the substrate, filling the various contact openings 84a, ..., 84g and making contact with the underlying semiconductor regions formed in silicon layer 20. Then conductive layer 90 is conventionally masked, the masking layer is patterned, and layer 90 is etched to define electrical contacts 90a, ..., 90g.

Then in Fig. 6 a conventional passivation layer of e.g. plasma nitride material is formed overlying electrical contacts 90a, ..., 90g. Passivation layer 96 is 0.5 to 2.5 micrometers thick.

Overlying passivation layer 96, an epoxy material layer 98 is conventionally deposited 25 to 250 micrometers thick. This epoxy material 98 is e.g. a high performance epoxy resin composition that is thermally conductive (such as silver epoxy).

Next a "cap" (plate) 100 is affixed to epoxy layer 98 which is then cured, bonding cap 100 to passivation layer 96. Cap 100 is about 500 micrometers thick and is e.g. undoped silicon. A single cap 100 covers the entire wafer which includes substrate 10 and silicon layer 20. Other bonding materials and processes other than epoxy may be used to affix cap 100. Cap 100 achieves thermal conductivity through epoxy layer 98 and also provides sufficient mechanical support for the substrate 10, silicon layer 20, and the active transistor regions and interconnect formed thereon.

Next in Fig. 7, the backside surface of substrate

10 is partially removed by grinding, etching, or CMP (chemical-mechanical polishing) so that the total thickness of substrate 10 and/or silicon layer 20 is in the range of 5 to 100 microns. This is in contrast to the original total thickness of structures 10 and 20 of about 500 microns. (Again, these dimensions are illustrative and not limiting.) The goal is to reduce the thickness of substrate 10 and silicon layer 20 to a minimum necessary for electrical functioning of the transistors formed therein. The removing step reduces the thickness of substrate 10 so that the bottom portion of each of trenches 72a, ..., 72e is exposed, and thereby the insulative material formed in each of these trenches is exposed at the backside surface of substrate 10. This achieves full electrical isolation of each portion of substrate 10. It is to be understood that in this case the attachment of heat sink cap 100 is done prior to the removing step to ensure that the substrate, after the removing step, remains in one integrated piece. Conventional masking, implantation, and annealing steps may be added to this process, as desired to form N+ or P+ contacts on the backside surface of substrate 10 for subsequent metal layer 104.

Next in Fig. 8, the backside surface of substrate 10 is metallized by a conventional sputtering or evaporative process to form a metal layer 104 (aluminum) thereon having a thickness of e.g. 0.15 to 1.5 micrometers. Then metal layer 104 is conventionally covered with a mask layer, the mask layer is patterned, and metal layer 104 then etched to define backside contact pads 104a, 104b on the backside surface of substrate 10. Each of contact pads 104a, 104b is associated with a selected portion of the integrated circuit die as defined by the trenches 72a, ..., 72e. Of course each portion of the die need not

have a contact pad; contact pads 104a, 104b are only provided to those portions of the die which require same. (It is to be understood that conventionally some types of transistors do not require backside contacts.)

Next in Fig. 9, a protective/passivation layer 110 is deposited on the backside surface of substrate 10 overlying contact pads 104a and 104b. Then layer 110 is conventionally patterned to define openings 112a and 112b. Each opening 112a and 112b is associated with a particular electrical contact 90a, 90g on the upper side surface of silicon layer 20, as shown.

Next in Fig. 10, a deep silicon etch is undertaken through openings 112a and 112b to define vias 116a, 116b extending through substrate 10 and/or silicon layer 20 to expose the underside portions of electrical contacts 90a, 90g. This deep silicon etching step uses a wet or wet/dry or dry etching technique.

Vias 116a, 116b need only be wide enough to establish good electrical paths to contacts 90a, 90g and otherwise their dimensions in terms of width are not critical; neither is their cross-sectional shape critical. Then as shown in Fig. 10 the remaining portions of layer 110 may be conventionally stripped off or kept as a passivation layer.

Next in Fig. 11 by a plating step (electrodeposition), vias 116a and 116b are filled with a solderable metal (e.g. nickel, gold, copper) to define posts 124, 130 extending therefrom. In the same electrodeposition step, metal posts 126, 128 are deposited on metal contacts 104a, 104b.

Alternatively, posts 126, 128 are formed by screen printing the desired type of metal on respectively the backside 104, 104b interconnection leads to establish the desired thickness for the surface mount posts. The diameter of the surface mount posts may vary, depending on the particular application.

Next in Fig. 12, an (optional) passivation layer 136 is deposited over all exposed surfaces of the surface mount posts 124, 126, 128 and 130 to a thickness of 0.8 to 1.2 micrometers. Passivation layer 136 is e.g. polyamide or low temperature oxide.

Then portions of passivation layer 136 are removed (by masking and etching or other means, for instance CMP) from the bottom surfaces of each surface mount post 124, 126, 128, 130, so as to leave the post bottom surfaces exposed for soldering, such as to a printed circuit board. The height of the surface mount posts extending from the lower backside surface of substrate 10 is conventionally 10 to 300 micrometers, or any other height as needed depending on the mounting application.

In Fig. 12 all of the electrical interconnections to outside of the chip are provided on the backside surface of substrate 10 by the surface mount posts 124, 126, 128 and 130.

Subsequently (not shown) the wafer is scribed into individual integrated circuit die along predescribed scribe lines which are for instance adjacent to dielectrically filled trenches. Thus as a result of the scribing step, the various integrated circuit die are already packaged by the top side cap 100 and the bottom side passivation layer 136; hence no further packaging is needed.

Flip Chip Embodiment

In the flip chip embodiment, the initial processing steps are identical to those shown in Figs. 1 to 5 for the surface mount embodiment, resulting in the structure of Fig. 13. Again, the flip chip embodiment is not limited to semiconductor devices of the type shown. The structure of Fig. 13 is identical to that of Fig. 5, except that in Fig. 13 the next step is that passivation layer 160 (which is similar in

material and thickness to passivation layer 96 in Fig. 6) is masked using a mask layer (not shown) which is patterned, with subsequent etching to define contact openings 164a, 164b, therethrough. Contact openings 164a, 164b, expose a portion of the underlying electrical contacts 90a, 90g. The goal in this embodiment is to define both substrate frontside and backside electrical contacts; openings 164a, 164b define the frontside contact openings.

Next in Fig. 14, silicon (or other suitable material) heat sink cap 172 is provided, having formed thereon (prior to assembly to the substrate 10) metal (aluminum or a solderable material) interconnect structures 176a, 176b. Interconnect structures 176a, 176b include interconnect lines on the surface of cap 172 which faces contacts 90a, 90b; these interconnect lines have a thickness of e.g. 10 to 50 micrometers. Cap 172 is electrically insulated on all surfaces by e.g. oxide dielectric layer 175. Interconnect structures 176a, 176b are then conventionally soldered or sintered to underlying contacts 90a, 90g. This electrical contact can be provided by any other conventional method.

Cap 172 is attached to the underlying structure by a high performance thermally conductive (and electrically insulative) epoxy resin layer 168 (or other high performance adhesive) formed on passivation layer 160 to a thickness of 25 to 250 micrometers. Adhesive layer 168 is prevented from fouling the electrical interconnections (between elements 176a, 176b and 90a, 90b) by masking and etching the adhesive layer 168 or by polishing it away from the interconnections. For instance, adhesive layer 168 is initially formed in a thick layer covering structures 176a, 176b, then etched back to expose the ends of structures 176a, 176b using a wet or dry etch.

It is to be understood that cap 172 serves as a heat sink and supports contact structures 176a, 176b which connect through vias extending through cap 172 to form interconnect contacts 174a, 174b on the opposite surface of cap 172. These interconnect contacts 174a, 174b are suitable for attachment to an underlying supporting conventional flip chip-type back plate (not shown) providing mechanical support and electrical bonds thereto.

Next in Fig. 15, (similar to Fig. 7) the backside surface of substrate 10 is polished or etched away to expose the lower portions of dielectrically insulated trenches 72a, ..., 72e. Again, the total thickness of substrate 10 and silicon layer 20 is minimized by this removing step to that needed for proper electrical functioning. Next in Fig. 16, backside contacts 178a, 178b are formed, similar to contacts 104a, 104b in Fig. 8. Next in Fig. 17, backside passivation layer 186 is deposited to a thickness of e.g. 0.5 to 2.5 micrometers using oxide or nitride or an oxide-nitride "sandwich" material over the backside surface of substrate 10 and initially over contact areas 178a and 178b, but is then removed from the exposed surfaces by use of a mask which is then patterned, and etching away of the unneeded portions of passivation layer 186. This exposes the bonding area of the power device drain contact 178a and a collector type drain contact 178b if desired. (Again the use of the backside contact depends on the nature of the associated semiconductor devices). Thus the flip chip configuration of Fig. 17 provides both frontside substrate electrical contacts 174a, 174b through cap 172 and also backside contacts 178a, 178b. The frontside leads are beam or tunnel lead structures or types to the transistors.

Again, after the steps of Fig. 17, the entire wafer is conventionally scribed along predetermined

scribe lines (not shown); thus as a result of scribing the chip is complete (packaged), advantageously without any need for further packaging steps.

Diamond Film Passivation Layer Embodiment

The above-described flip chip type and surface mount embodiments use conventional silicon dioxide or nitride as the dielectric insulation and passivation layer between the semiconductor wafer itself and the heat sink plate. These materials are known to provide relatively poor heat conduction, due to for instance the very low thermal conductivity of silicon dioxide of approximately 2 W/mK. In contrast, diamond film (which is also a good dielectric insulating material) provides thermal conductivities of about 2,000 W/mK. Also diamond is well known to be chemically inert, and due to its having the densest crystal lattice of any known material, the diffusion of other elements into diamond is very low. Thus diamond is not only a good dielectric insulator with excellent thermal conductivity but it is also a material which serves effectively as a passivation layer, providing good corrosion protection.

It has been determined in accordance with invention that diamond film has the best combination of thermal conductivity and electrical resistivity of available materials. Other materials such as aluminum nitride, aluminum oxide, or silicon carbide also provide high dielectric insulation but much less thermal conductivity than diamond. The only materials providing thermal conductivity similar to that of diamond film are electrically conductive metals such as copper and silver, which are not useful for passivation.

It is well known to provide chemical vapor deposition (CVD) of diamond film deposited at

temperatures of 600° to 950°C and at sub-atmospheric pressures. Typically methane or acetylene is used as the carbon source with significant partial pressure of atomic hydrogen. Excitation sources used include microwave and radio frequency plasmas, hot filament and thermal plasmas and combustion flames.

It has also been known to achieve a diamond deposition at temperatures below 600°C, for instance by using other process gas mixtures such as adding rare gases to the commonly utilized mixtures of carbon containing gases and hydrogen, mixtures of alcohols and water, halogenated gases and other gaseous combination. Typically growth rates of about 0.2 micrometers per hour have been achieved at deposition temperatures of about 400°C.

Methods for depositing diamond film in accordance with the present invention include low temperature microwave plasma assisted CVD. An alternative is an arc jet CVD process. It is known to pattern diamond films using conventional oxygen-based RIE (reactive ion etching) processes, as are well known in semi-conductor fabrication.

Thus in accordance with the invention for the above-described surface mount embodiment, a diamond film formed by one of the above described processes (or any other process) is substituted for passivation layer 96. The diamond film is formed to be a layer e.g. approximately 0.5 to 10 micrometers thick (but this is not limiting). Then the next substitution is, instead of using an ordinary epoxy material layer 98, a thermally conductive adhesive such as commercially available silver epoxy is used to bond the plate 100 to the diamond film. All other processing steps are as described above for this embodiment.

Similarly, for the above-described flip chip type embodiment, passivation layer 160 is a CVD (or other

type) diamond film approximately 0.5 to 10 micrometers thick (again this dimension is not limiting). This diamond film is, as described above for the non-diamond film flip chip type embodiment, masked using a mask layer to pattern it to define the contact openings 164A, 164B therethrough. The remaining of the processing is as described above, using a thermally conductive (but electrically insulative) high performance adhesive to bond the heat sink cap 172 to the diamond film passivation layer 160. Thus the process steps in terms of structure are similar to those described above for the non-diamond film flip chip type embodiment, except for the presence of the diamond film passivation layer material.

The above description is illustrative and not limiting; it will be understood by one of ordinary skill in the art that further modifications will be apparent in view of this disclosure, and fall within the scope of the appended claims.

We Claim:

1. An integrated circuit comprising:

A semiconductor substrate having a principal surface;

a plurality of semiconductor devices formed in the substrate;

a pattern of conductive lines formed overlying the principal surface and in electrical contact with the devices;

a diamond film at least partially overlying the pattern of conductive lines;

a thermally conductive plate bonded to the diamond film and overlying the pattern of conductive lines; and

a plurality of insulated trenches extending from the principal surface of the substrate through the substrate and to an opposing backside surface thereof.

2. The integrated circuit of Claim 1, further comprising a plurality of electrically conductive contacts formed on the backside surface of the substrate, each conductive contact being in contact with a selected portion of the backside surface as defined by the plurality of trenches.

3. The integrated circuit of Claim 1, wherein a thickness of the substrate is less than about 50 micrometers.

4. The integrated circuit of Claim 1, further comprising a second pattern of conductive lines juxtaposed to the plate and in electrical contact with the first pattern.

5. The integrated circuit of Claim 1, wherein the substrate defines a plurality of conductive vias extending from the principal surface thereof to the backside surface thereof, each via being in electrical contact on the principal surface with a portion of the pattern of conductive lines, and each via forming an electrical contact on the backside surface.

6. The integrated circuit of Claim 5, wherein the electrical contacts on the backside surface are each a post extending from the backside surface.

7. The integrated circuit of Claim 1, wherein the diamond film has a thickness in the range of 0.5 to 10 micrometers.

8. The integrated circuit of Claim 1, wherein the diamond film is bonded to the plate by a thermally conductive adhesive layer.

9. A method of forming an integrated circuit, comprising the steps of:

providing a semiconductor substrate having a principal surface;

forming a plurality of semiconductor devices in the substrate;

forming a plurality of trenches in the substrate extending from the principal surface thereof into the substrate to a particular depth;

forming a layer of insulating material in each of the trenches;

forming a pattern of conductive lines overlying the principal surface and in electrical contact with the devices;

forming a diamond film layer overlying the substrate;

bonding a thermal conductive plate to the diamond film layer and overlying the principal surface of the substrate; and

removing a portion of the substrate from a backside surface thereof opposing the principal surface, thereby exposing at least a bottom part of each of the trenches.

10. The method of Claim 9, further comprising the steps of:

forming a conductive layer on the backside surface; and

patterning the conductive layer into a plurality of contact regions, each contact region being in contact with a selected portion of the backside surface as defined by the plurality of trenches.

11. The method of Claim 9 wherein the step of removing leaves a remaining thickness of the substrate of less than about 100 micrometers.

12. The method of Claim 9, further comprising the step of forming a second pattern of conductive lines on a surface of the plate prior to the step of bonding;

wherein the step of bonding comprises electrically contacting portions of the second pattern to portions of the first pattern.

13. The method of Claim 9 wherein the step of bonding comprises applying a thermally conductive adhesive between the diamond film layer and the plate.

14. The method of Claim 9, further comprising the steps of:

forming a plurality of vias extending from the backside surface to the principal surface of the substrate, after the step of removing;

providing conductive material in each of the vias, the conductive material in each via being in electrical contact on the principal surface with a portion of the pattern of conductive lines, and the conductive material in each via forming an electrical contact on the backside surface.

15. The method of Claim 14, wherein the step of providing conductive material comprises forming a layer of the conductive material on the backside surface, and further comprising:

forming the layer of conductive material into a plurality of posts extending outward from the backside surface, each post being electrically connected to the conductive material in one of the vias.

16. The method of Claim 9, wherein the diamond film layer is formed to a thickness in a range of 0.5 to 10 micrometers.

AMENDED CLAIMS

[received by the International Bureau on 18 September 1995 (18.09.95); original claims 1,6-9,11,13 and 16 amended; new claims 17 and 18 added; remaining claims unchanged (4 pages)]

1. An integrated circuit comprising:

A semiconductor substrate having a principal surface and a thickness less than about 100 micrometers;

a plurality of semiconductor devices formed in the substrate;

a pattern of conductive lines formed overlying the principal surface and in electrical contact with the devices;

an electrically insulating film at least partially overlying the pattern of conductive lines;

a thermally conductive plate permanently bonded to the insulating film and overlying the pattern of conductive lines; and

a plurality of insulated trenches extending from the principal surface of the substrate through the substrate and to an opposing backside surface thereof.

2. The integrated circuit of Claim 1, further comprising a plurality of electrically conductive contacts formed on the backside surface of the substrate, each conductive contact being in contact with a selected portion of the backside surface as defined by the plurality of trenches.

3. The integrated circuit of Claim 1, wherein a thickness of the substrate is less than about 50 micrometers.

4. The integrated circuit of Claim 1, further comprising a second pattern of conductive lines juxtaposed to the plate and in electrical contact with the first pattern.

5. The integrated circuit of Claim 1, wherein the substrate defines a plurality of conductive vias extending from the principal surface thereof to the backside surface thereof, each via being in electrical contact on the principal surface with a portion of the pattern of conductive lines, and each via forming an electrical contact on the backside surface.

6. The integrated circuit of Claim 5, wherein the electrical contacts on the backside surface are each a post extending from the backside surface.

7. The integrated circuit of Claim 1, wherein the insulating film has a thickness in the range of 0.5 to 10 micrometers.

8. The integrated circuit of Claim 1, wherein the insulating film is bonded to the plate by a thermally conductive adhesive layer.

9. A method of forming an integrated circuit, comprising the steps of:

providing a semiconductor substrate having a principal surface;

forming a plurality of semiconductor devices in the substrate;

forming a plurality of trenches in the substrate extending from the principal surface thereof into the substrate to a particular depth;

forming a layer of insulating material in each of the trenches;

forming a pattern of conductive lines overlying the principal surface and in electrical contact with the devices;

forming an electrically insulating film layer overlying the substrate;

permanently bonding a thermal conductive plate to the insulating film layer and overlying the principal surface of the substrate; and

removing a portion of the substrate from a backside surface thereof opposing the principal surface, thereby exposing at least a bottom part of each of the trenches and reducing a thickness of the substrate to less than about 100 micrometers.

10. The method of Claim 9, further comprising the steps of:

forming a conductive layer on the backside surface; and

patterning the conductive layer into a plurality of contact regions, each contact region being in contact with a selected portion of the backside surface as defined by the plurality of trenches.

11. The method of Claim 9 wherein the step of removing leaves a remaining thickness of the substrate of less than about 50 micrometers.

12. The method of Claim 9, further comprising the step of forming a second pattern of conductive lines on a surface of the plate prior to the step of bonding;

wherein the step of bonding comprises electrically contacting portions of the second pattern to portions of the first pattern.

13. The method of Claim 9 wherein the step of bonding comprises applying a thermally conductive adhesive between the insulating film layer and the plate.

14. The method of Claim 9, further comprising the steps of:

forming a plurality of vias extending from the backside surface to the principal surface of the substrate, after the step of removing;

providing conductive material in each of the vias, the conductive material in each via being in electrical contact on the principal surface with a portion of the pattern of conductive lines, and the conductive material in each via forming an electrical contact on the backside surface.

15. The method of Claim 14, wherein the step of providing conductive material comprises forming a layer of the conductive material on the backside surface, and further comprising:

forming the layer of conductive material into a plurality of posts extending outward from the backside surface, each post being electrically connected to the conductive material in one of the vias.

16. The method of Claim 9, wherein the insulating film layer is formed to a thickness in a range of 0.5 to 10 micrometers.

17. The integrated circuit of Claim 1, wherein the insulating film is a diamond film.

18. The method of Claim 9, wherein the insulating film is a diamond film.

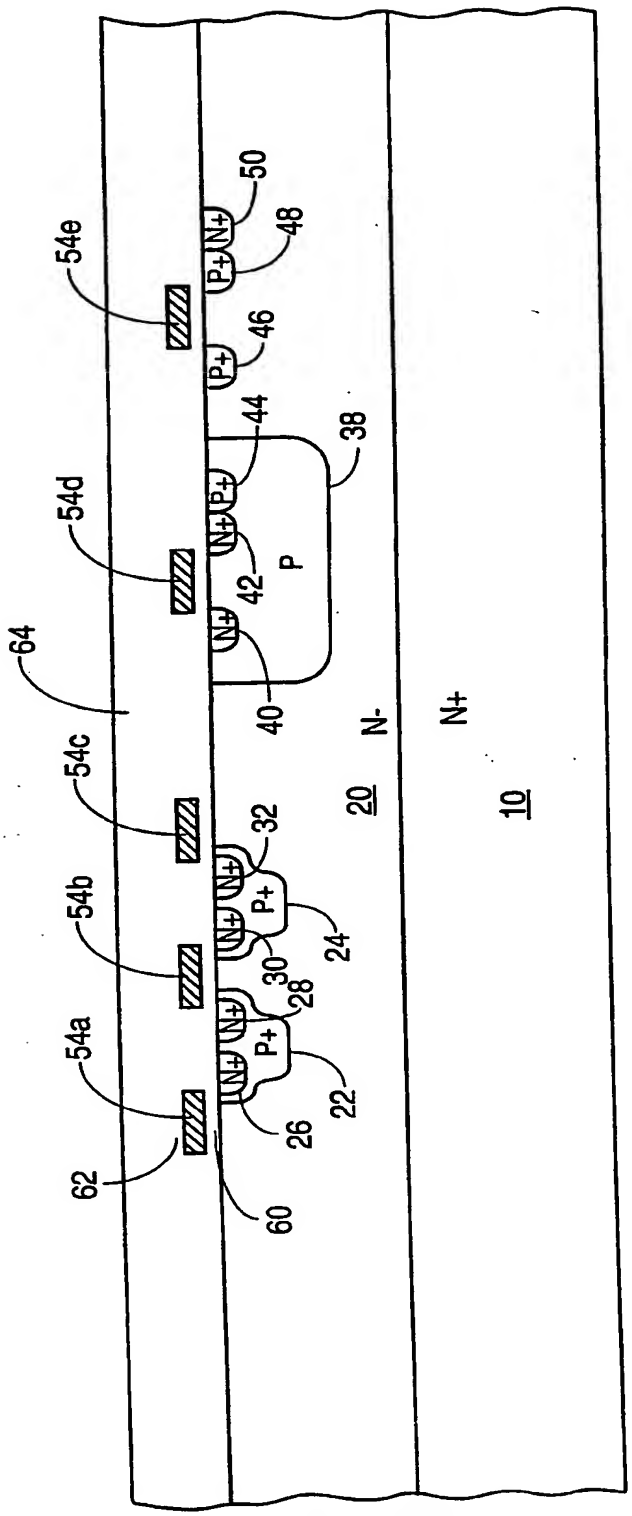
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Fig. 1

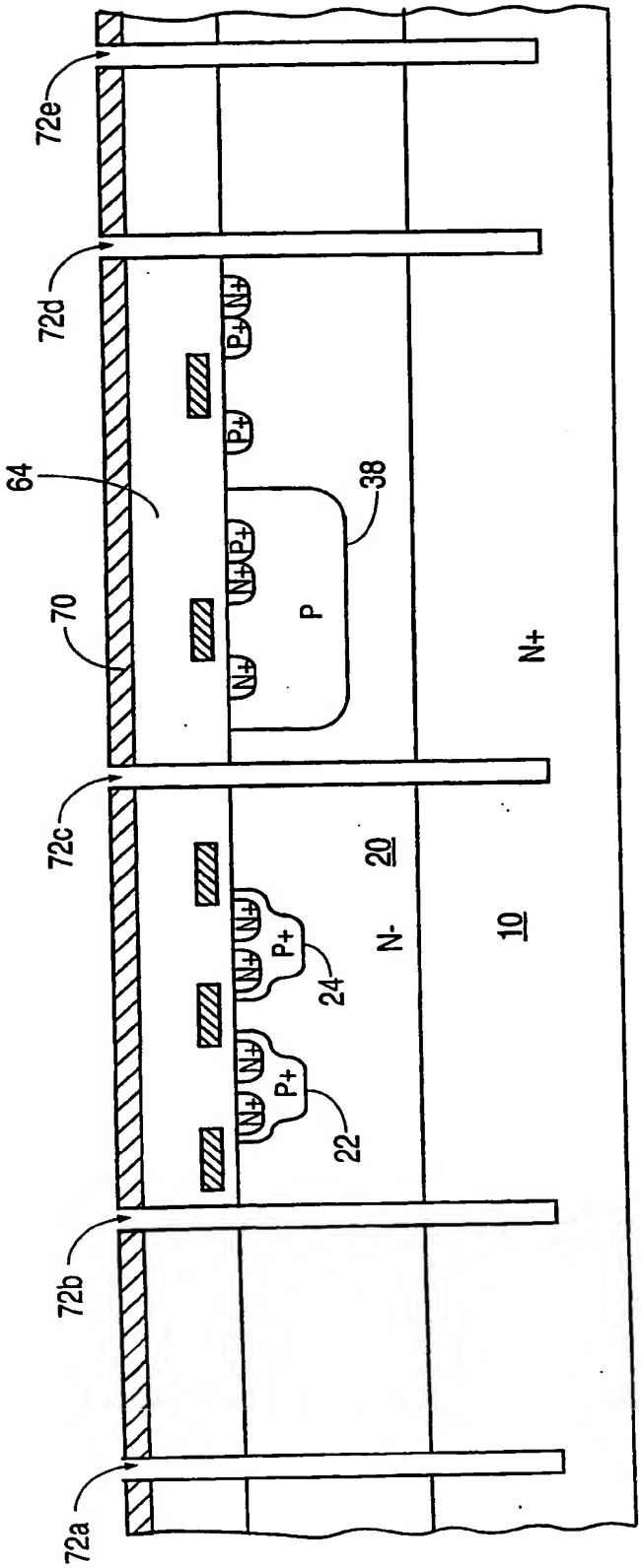

Fig. 2

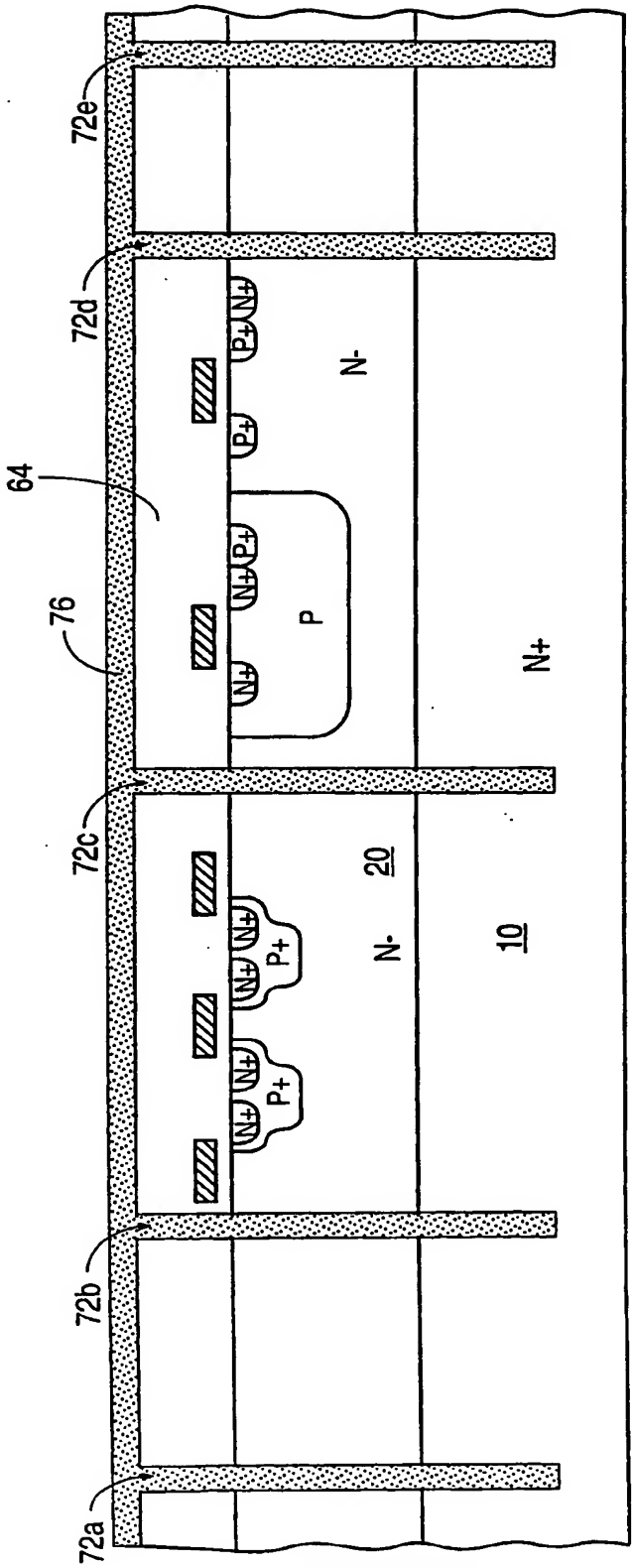

Fig. 3

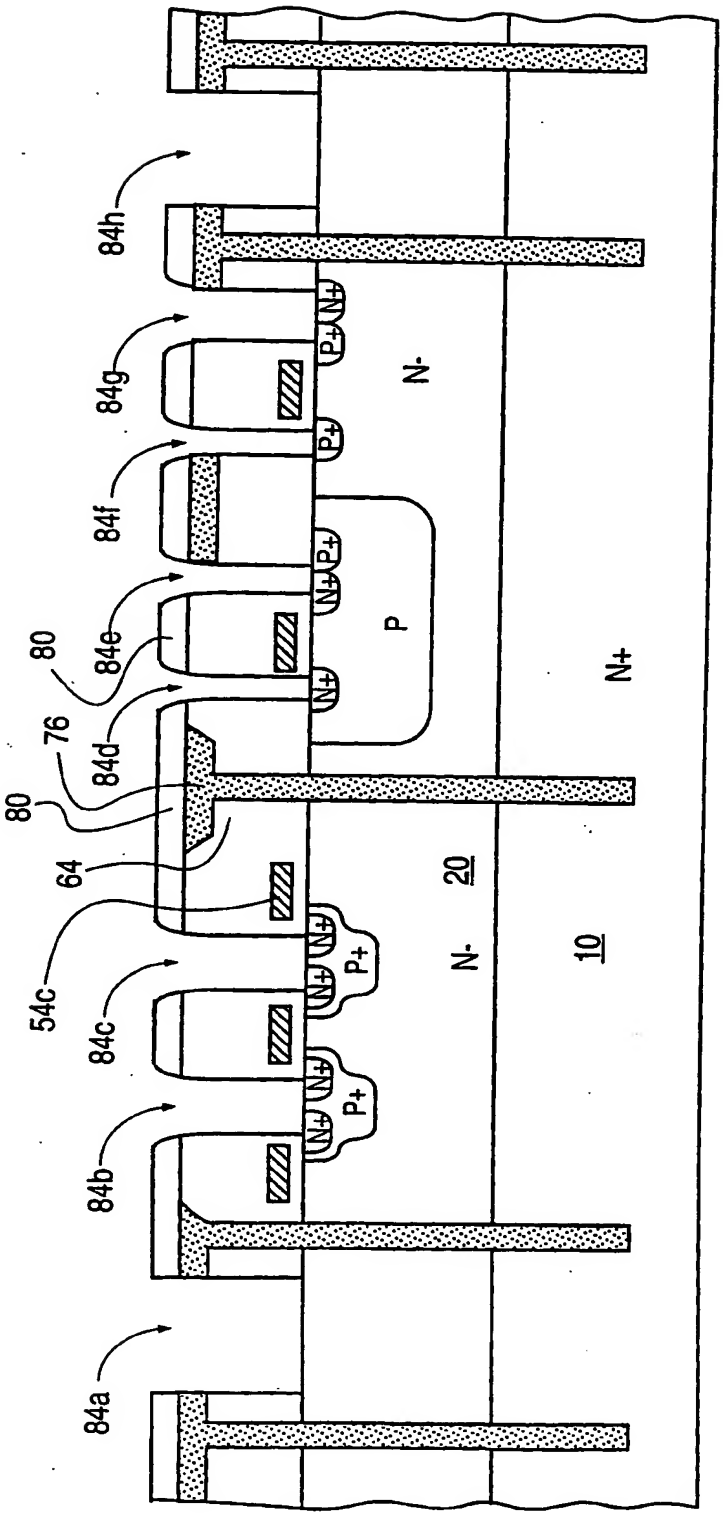

Fig. 4

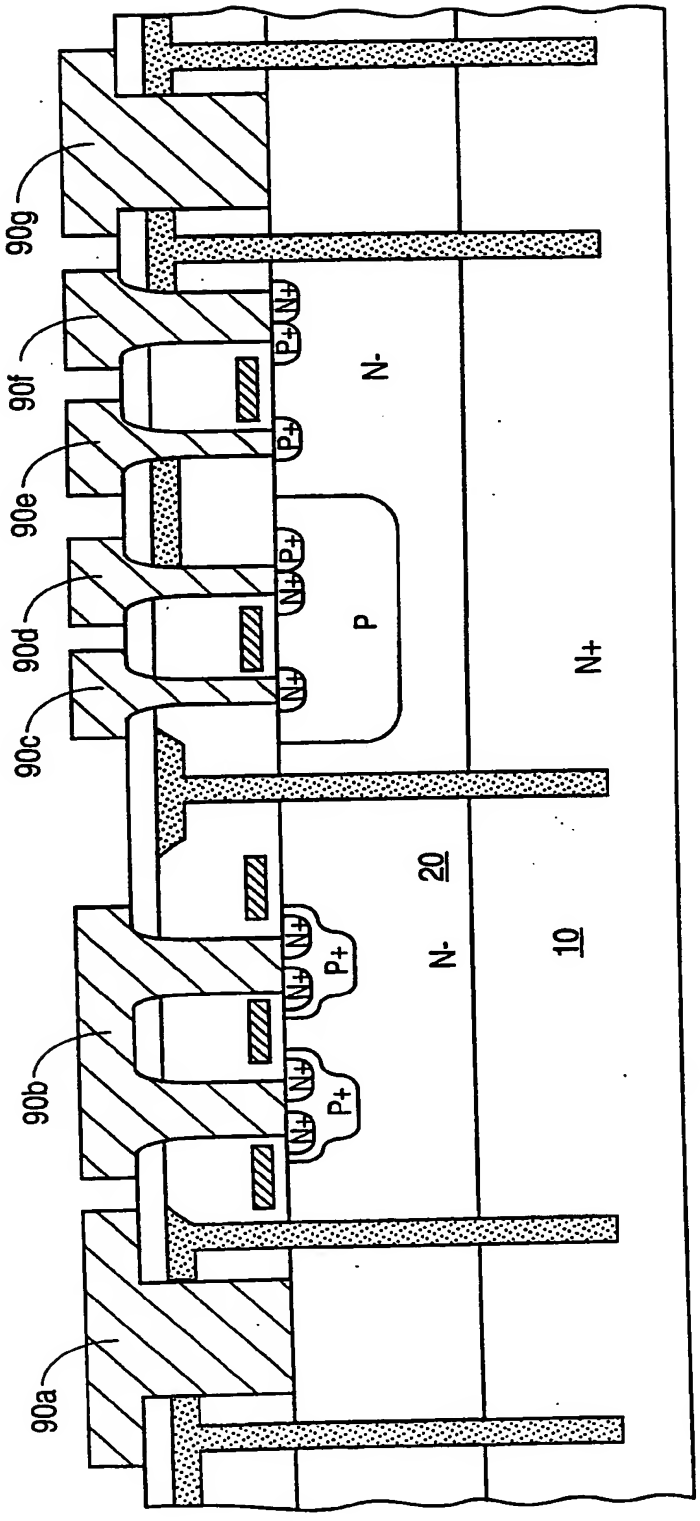

Fig. 5

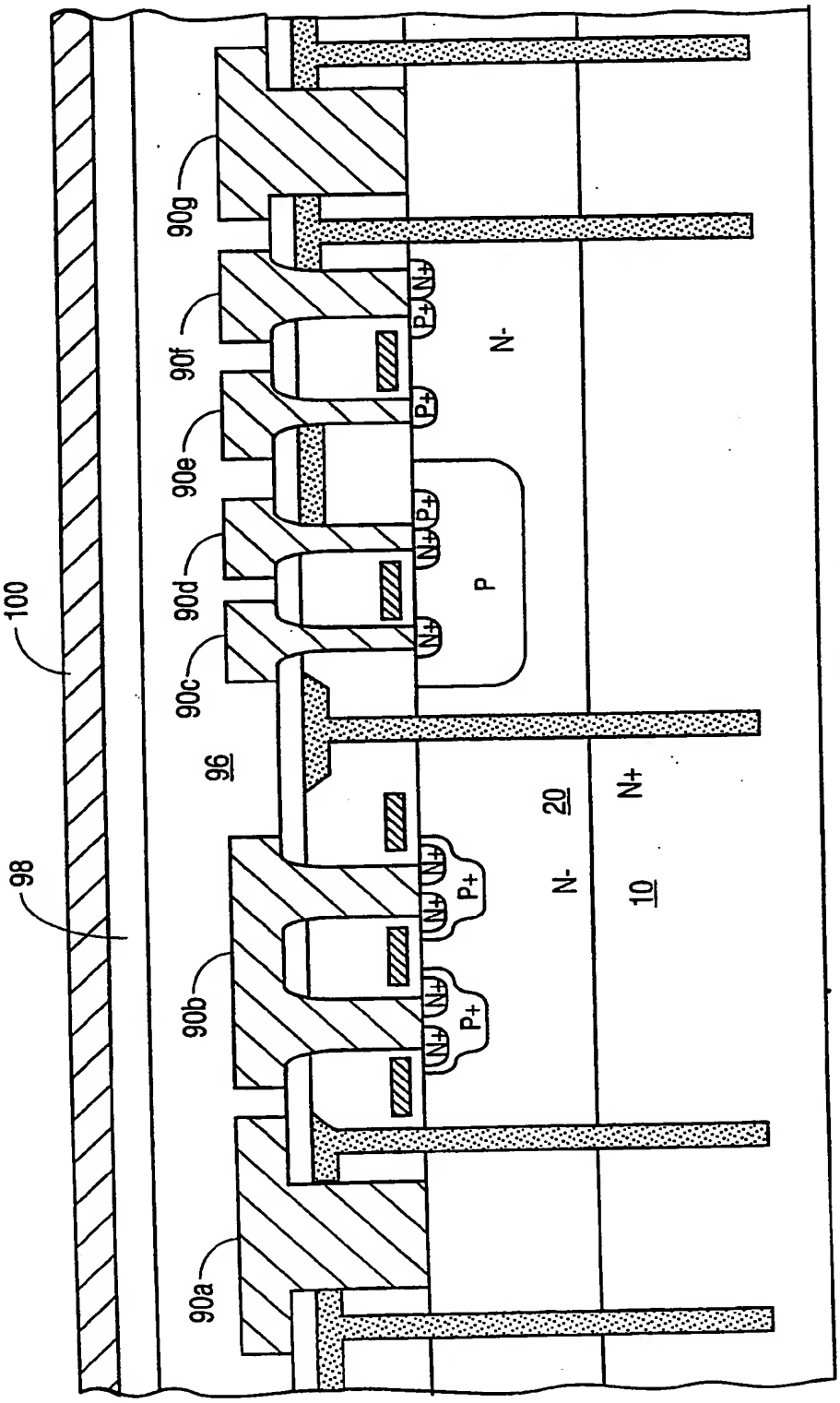

Fig. 6

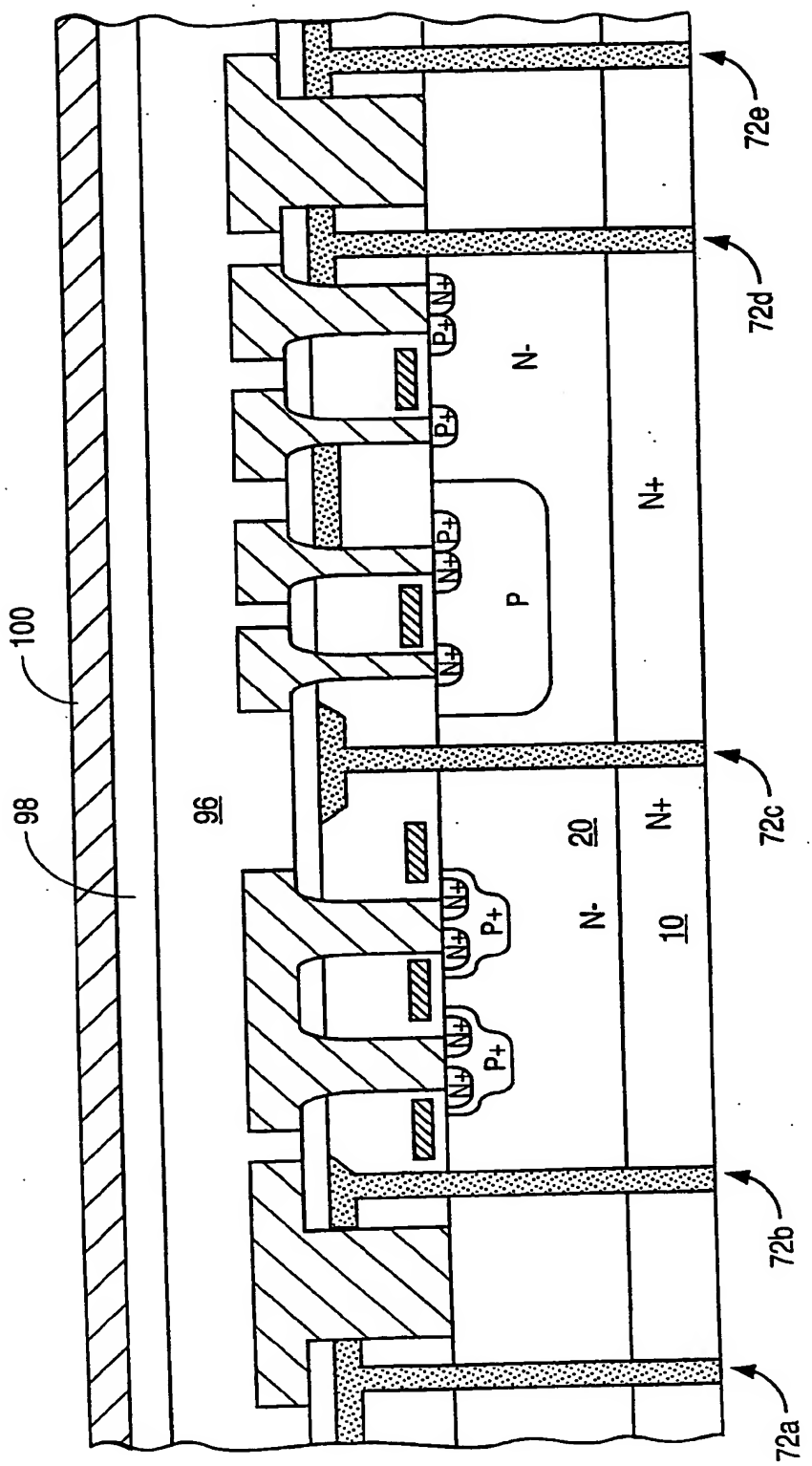

Fig. 7

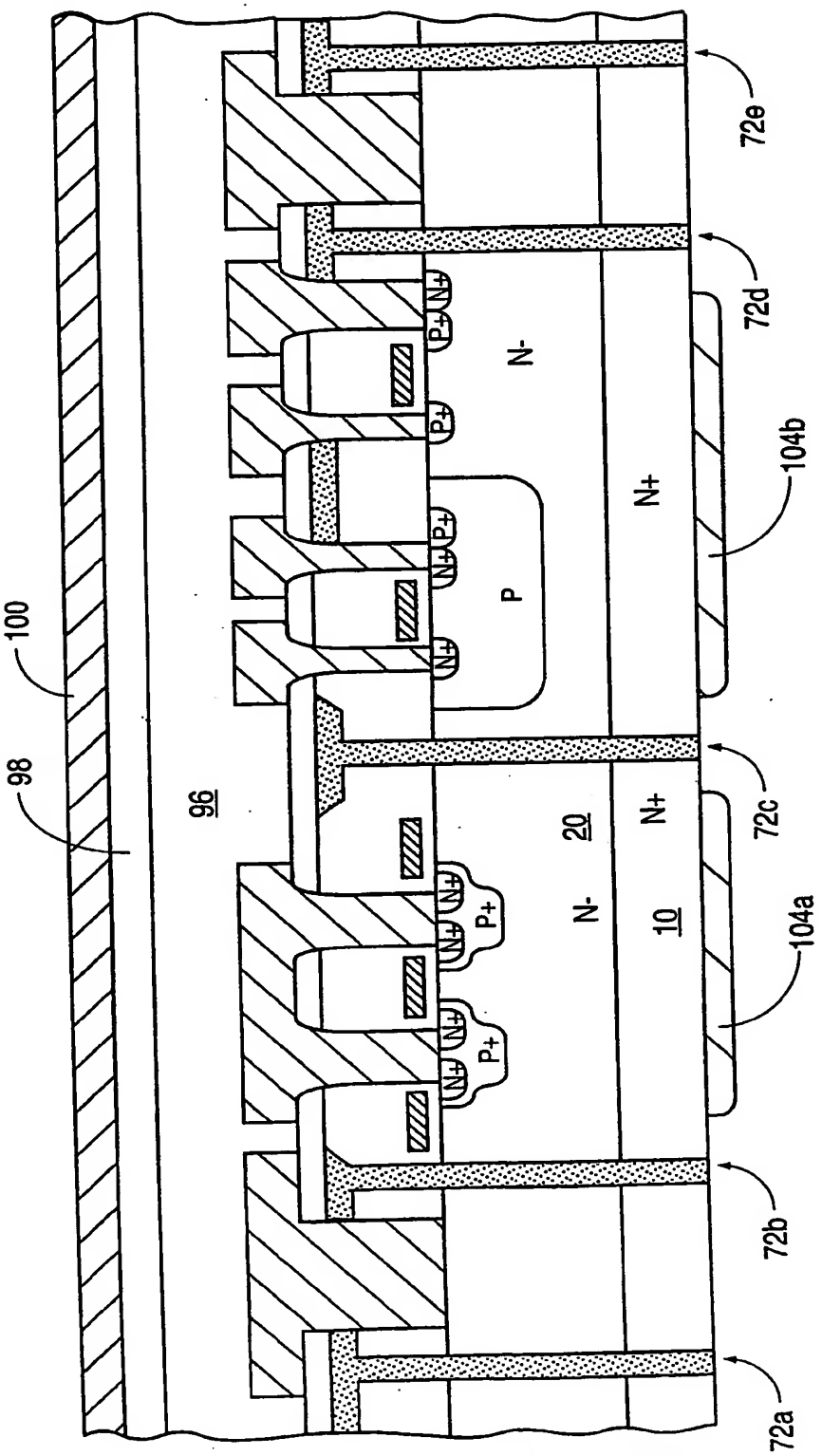

Fig. 8

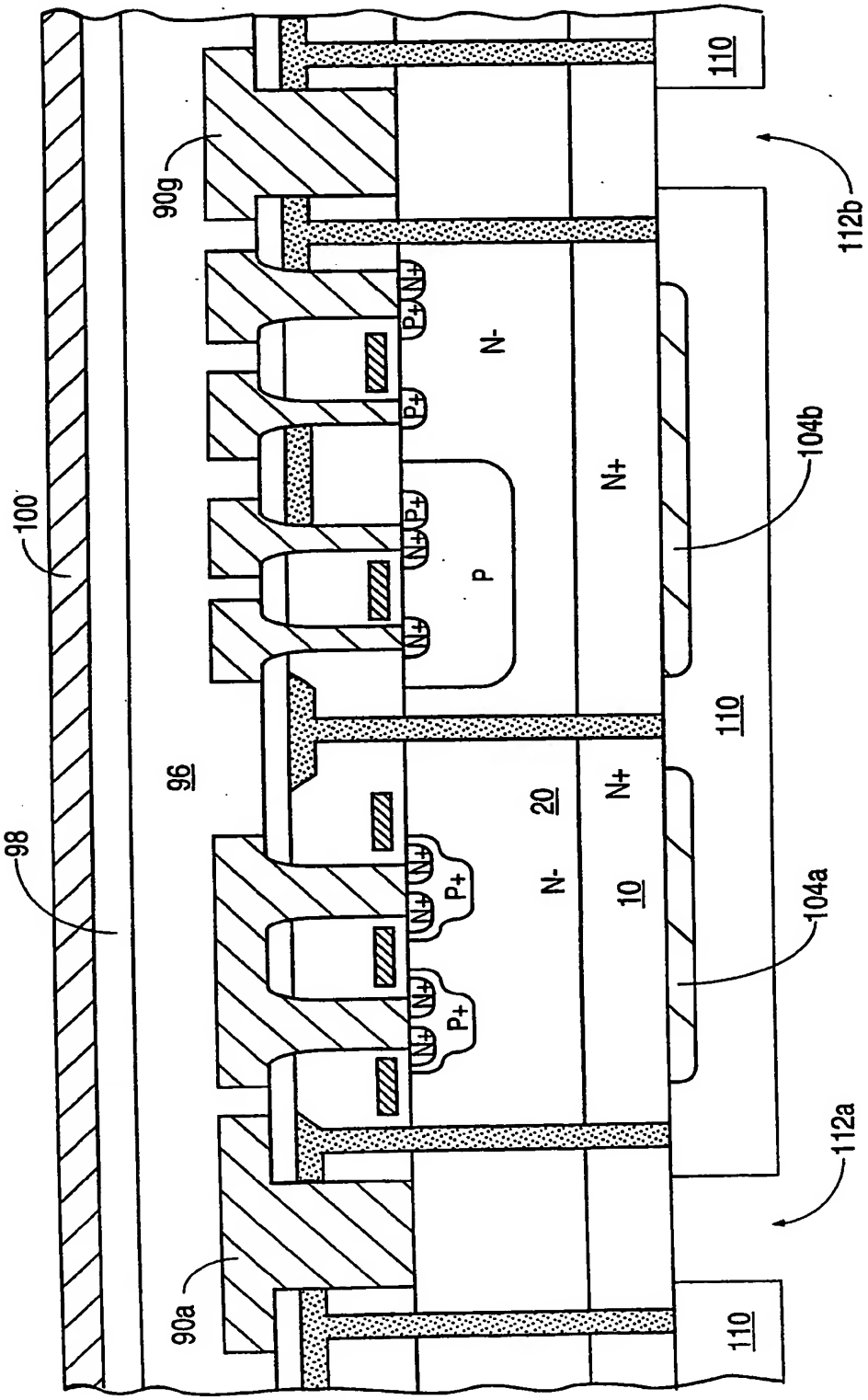
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Fig. 9

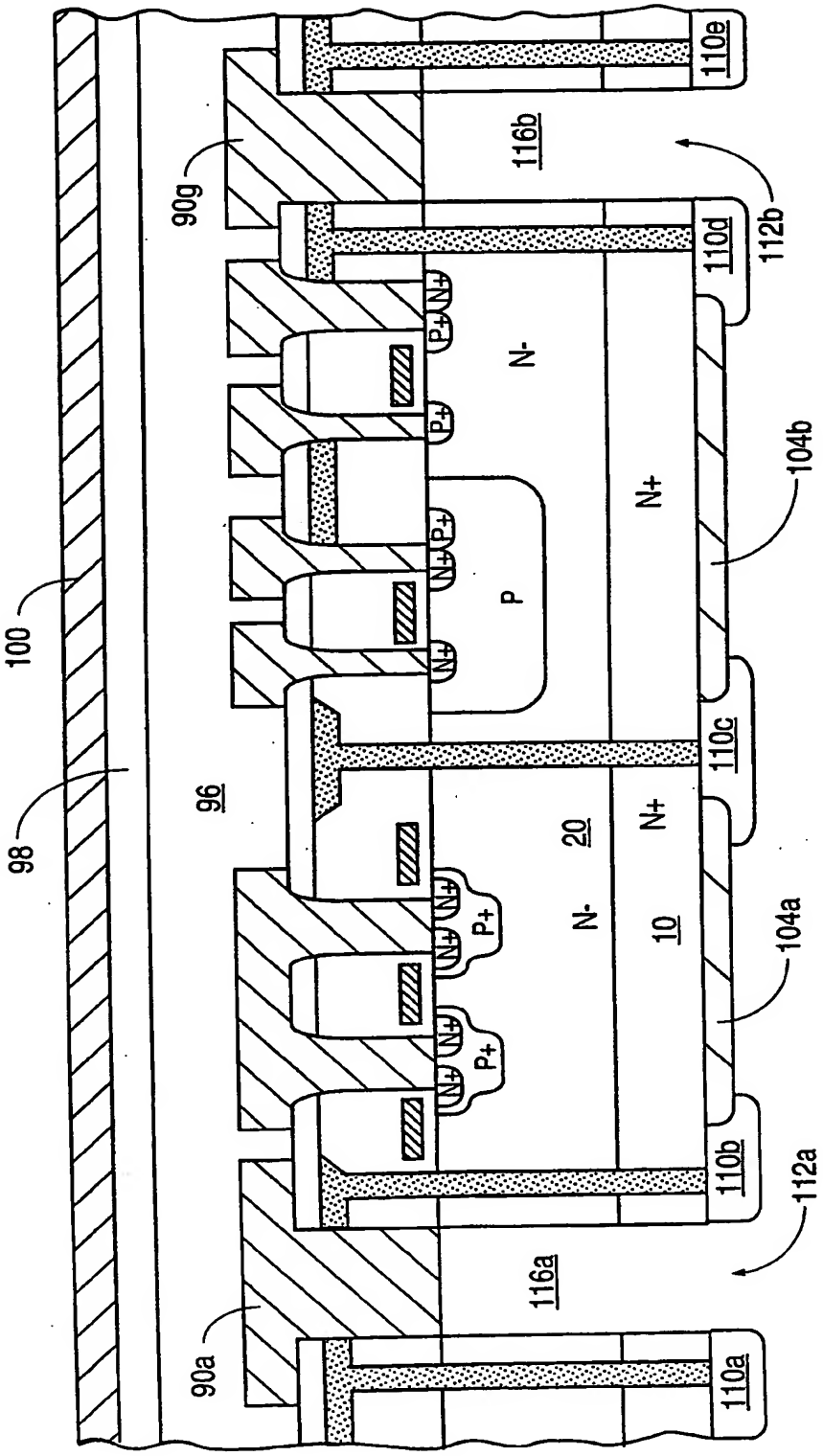
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Fig. 10

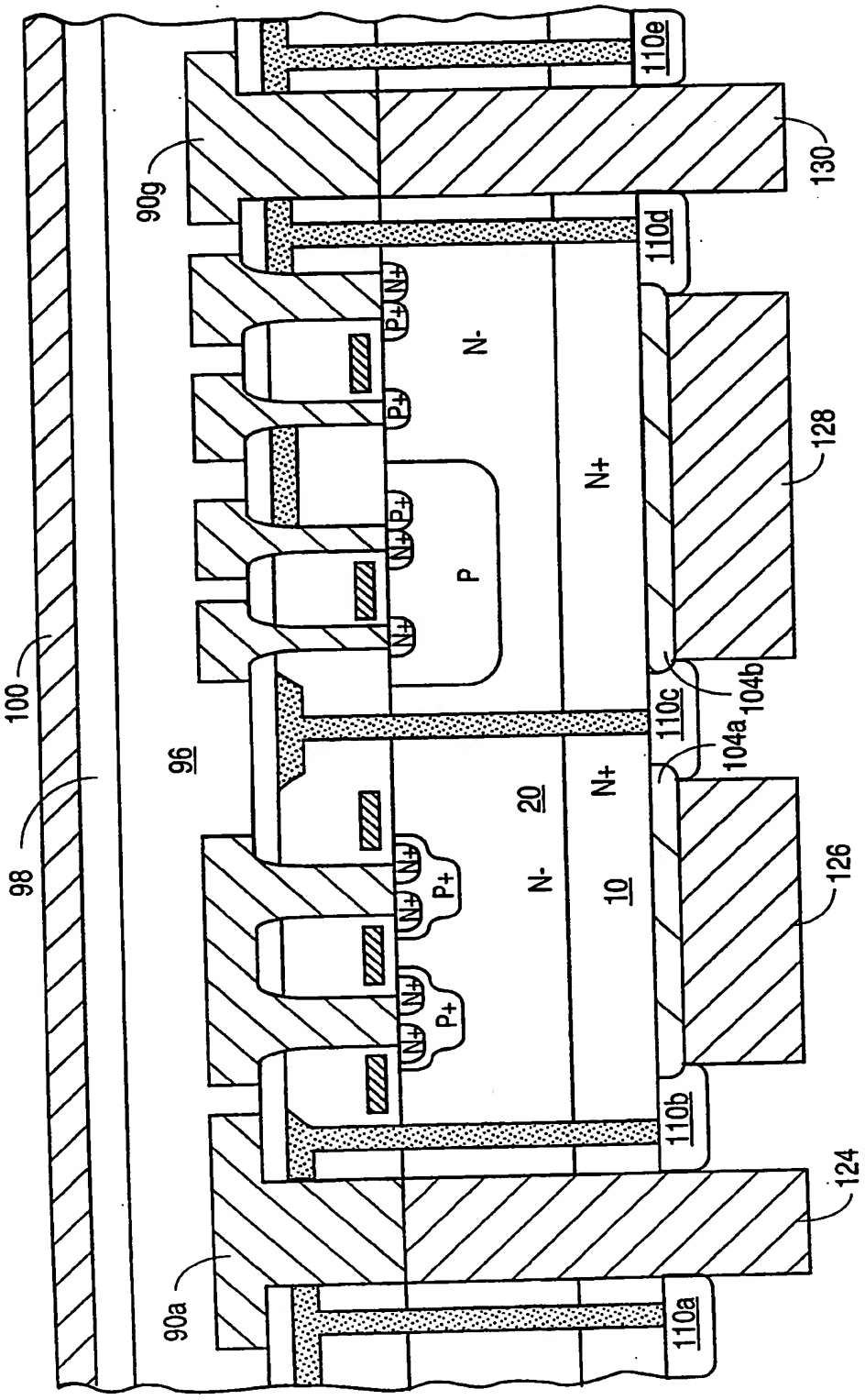
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Fig. 11

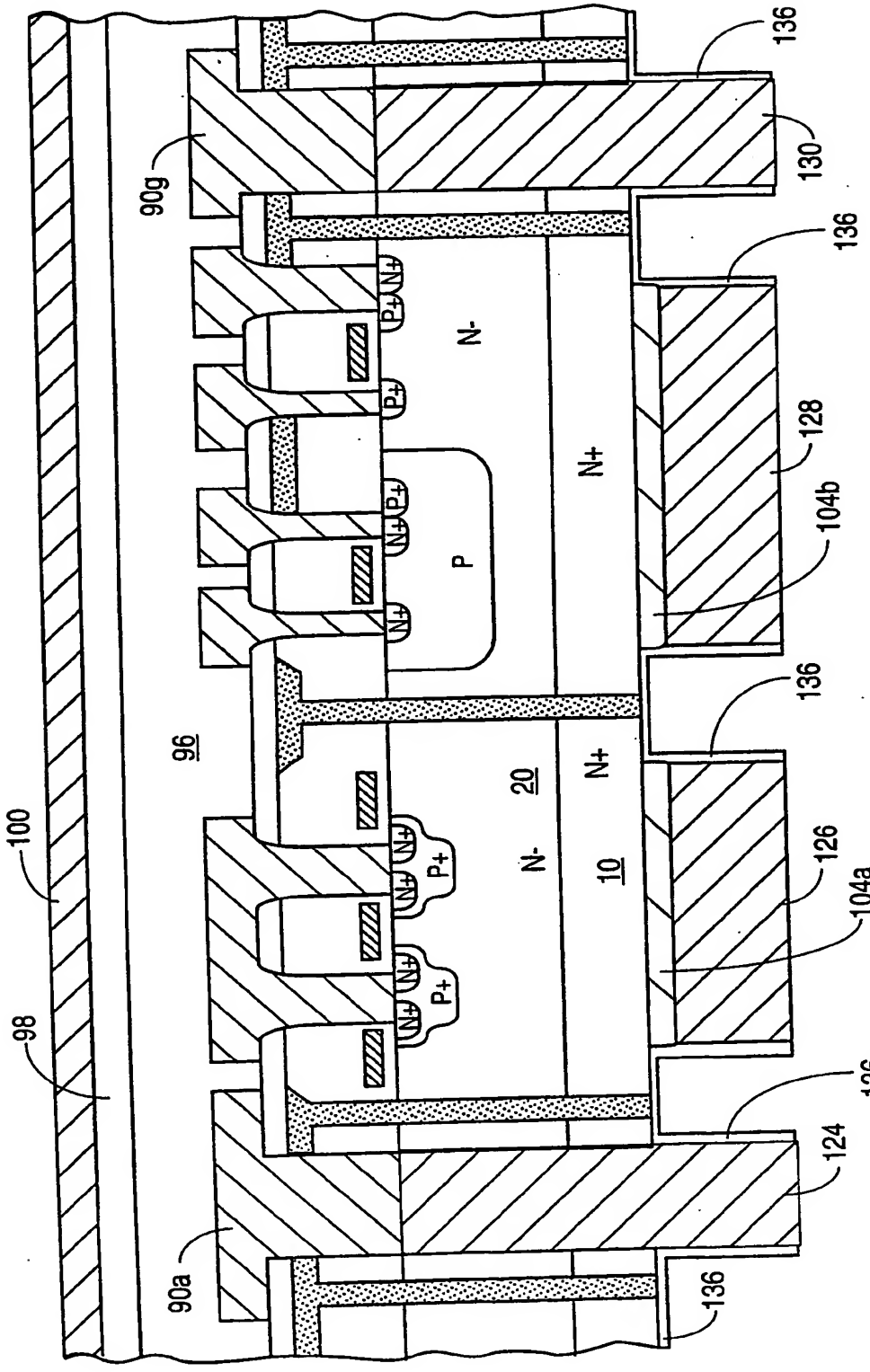
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Fig. 12

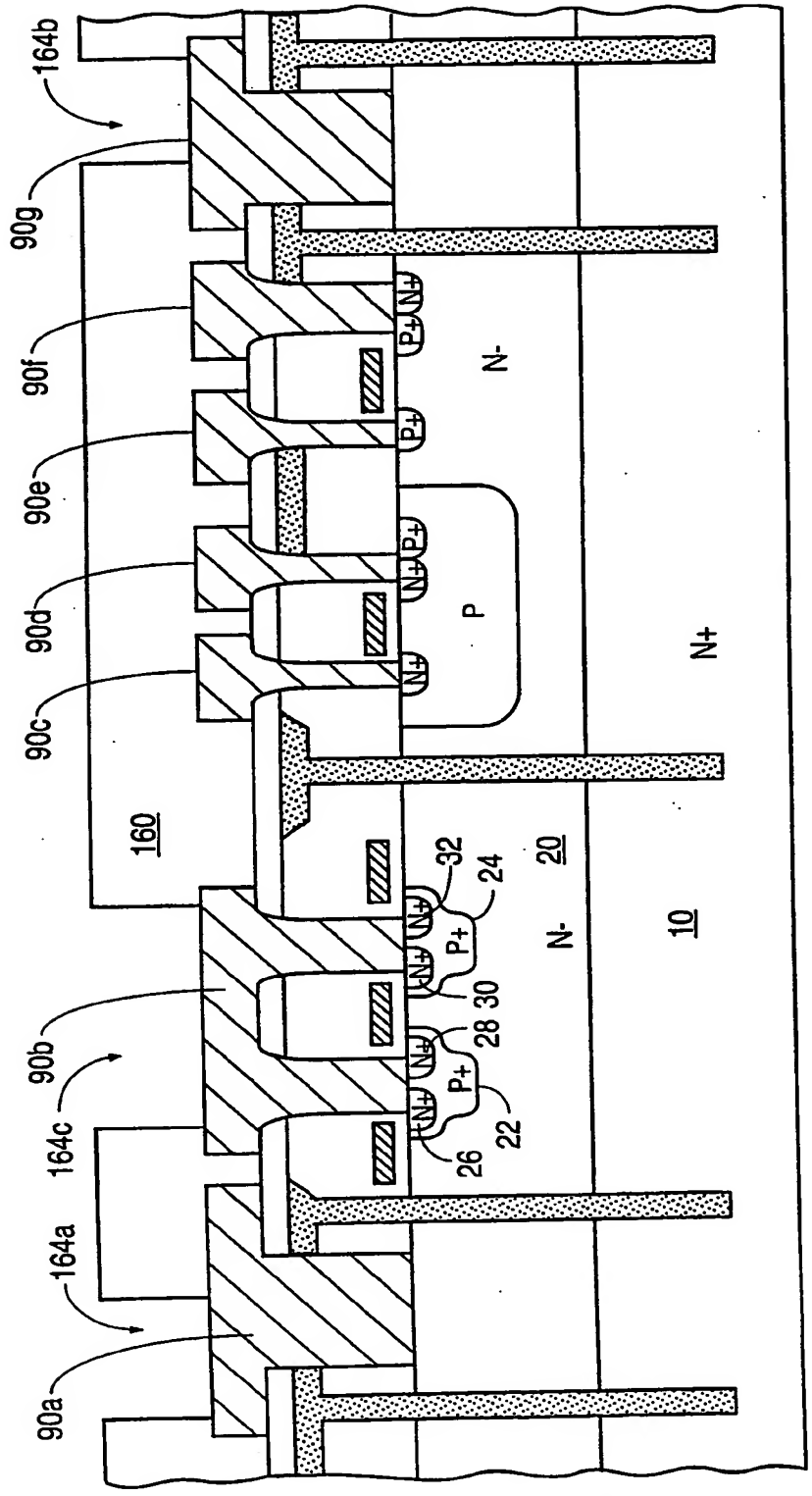
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Fig. 13

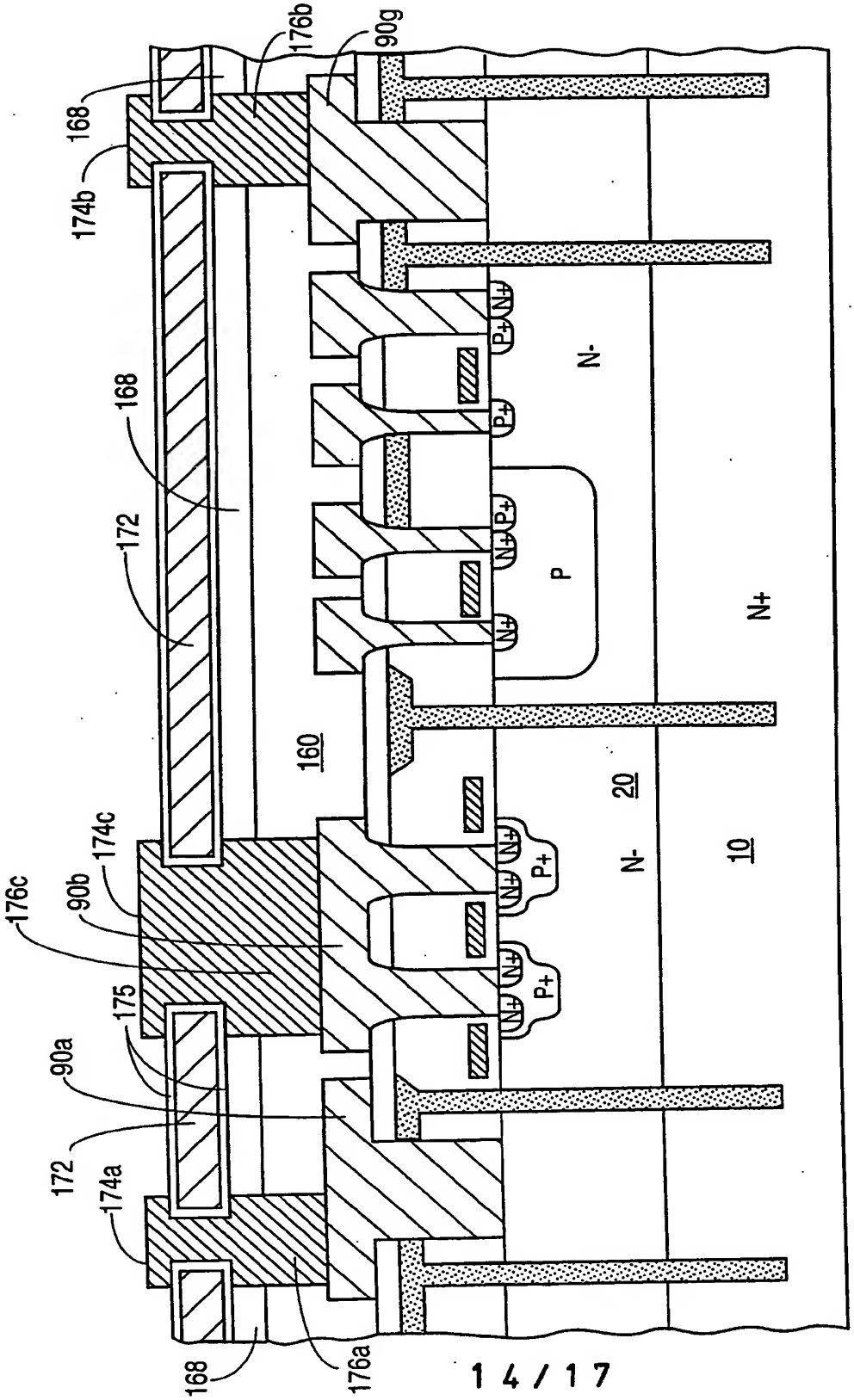
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Fig. 14

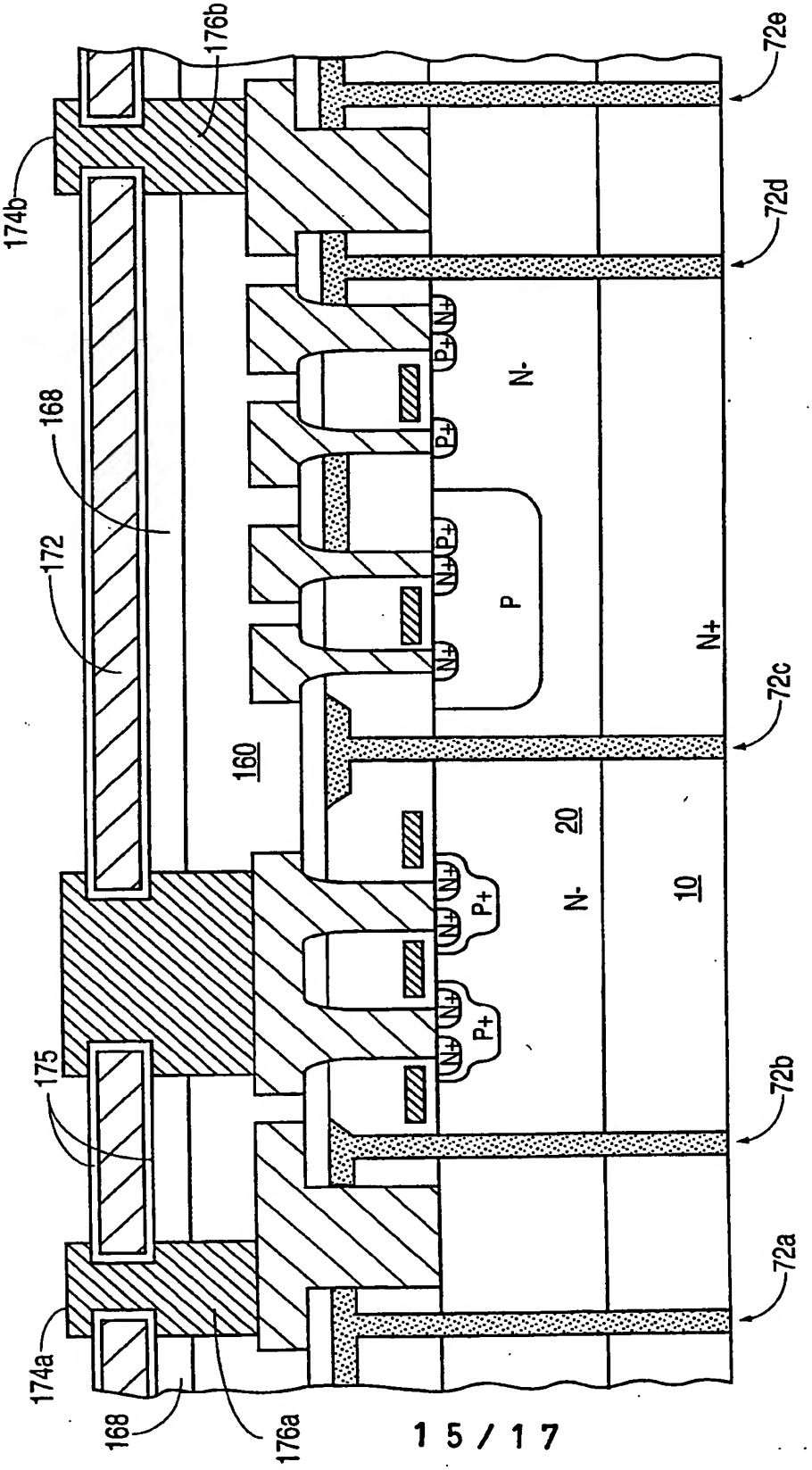
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Fig. 15

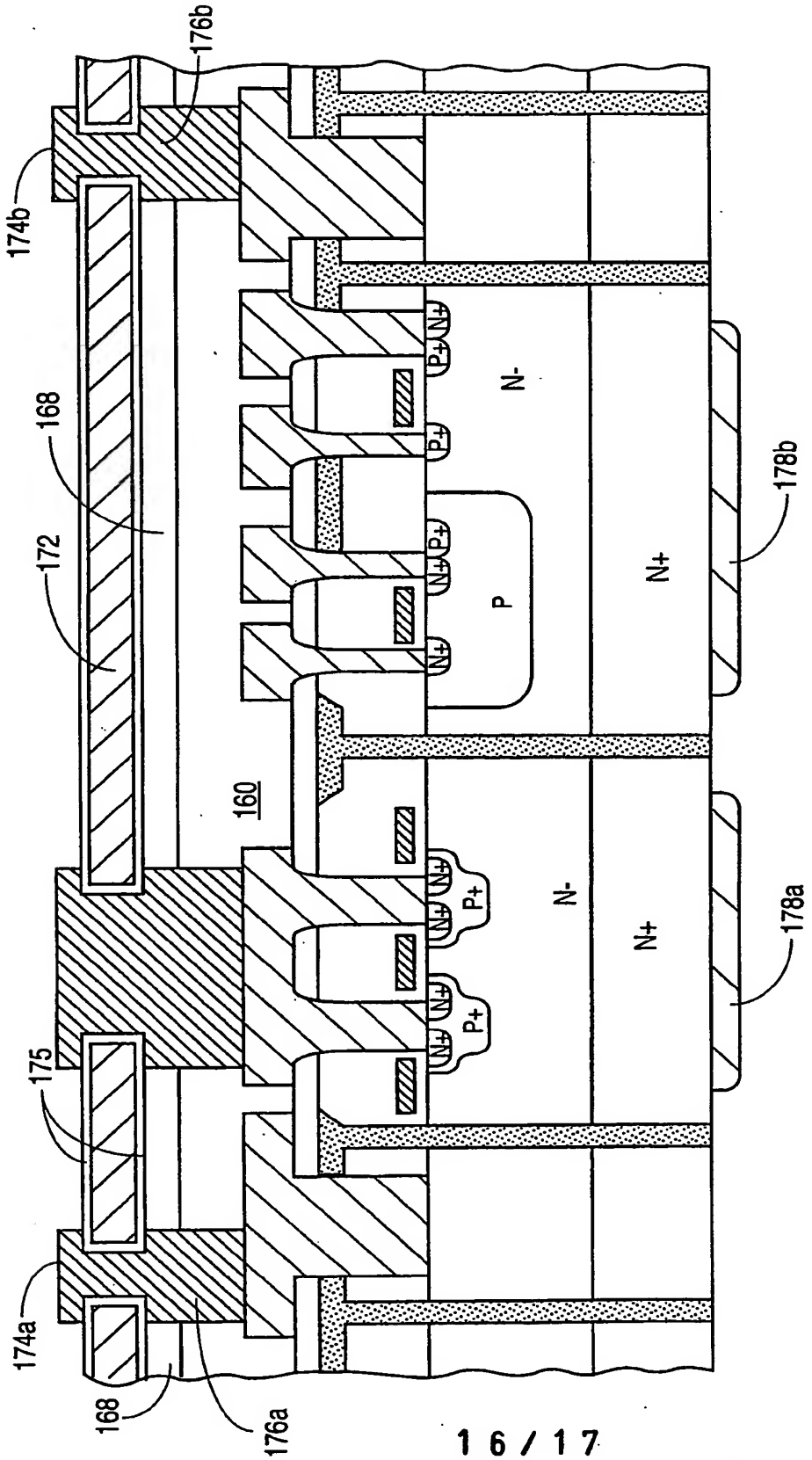
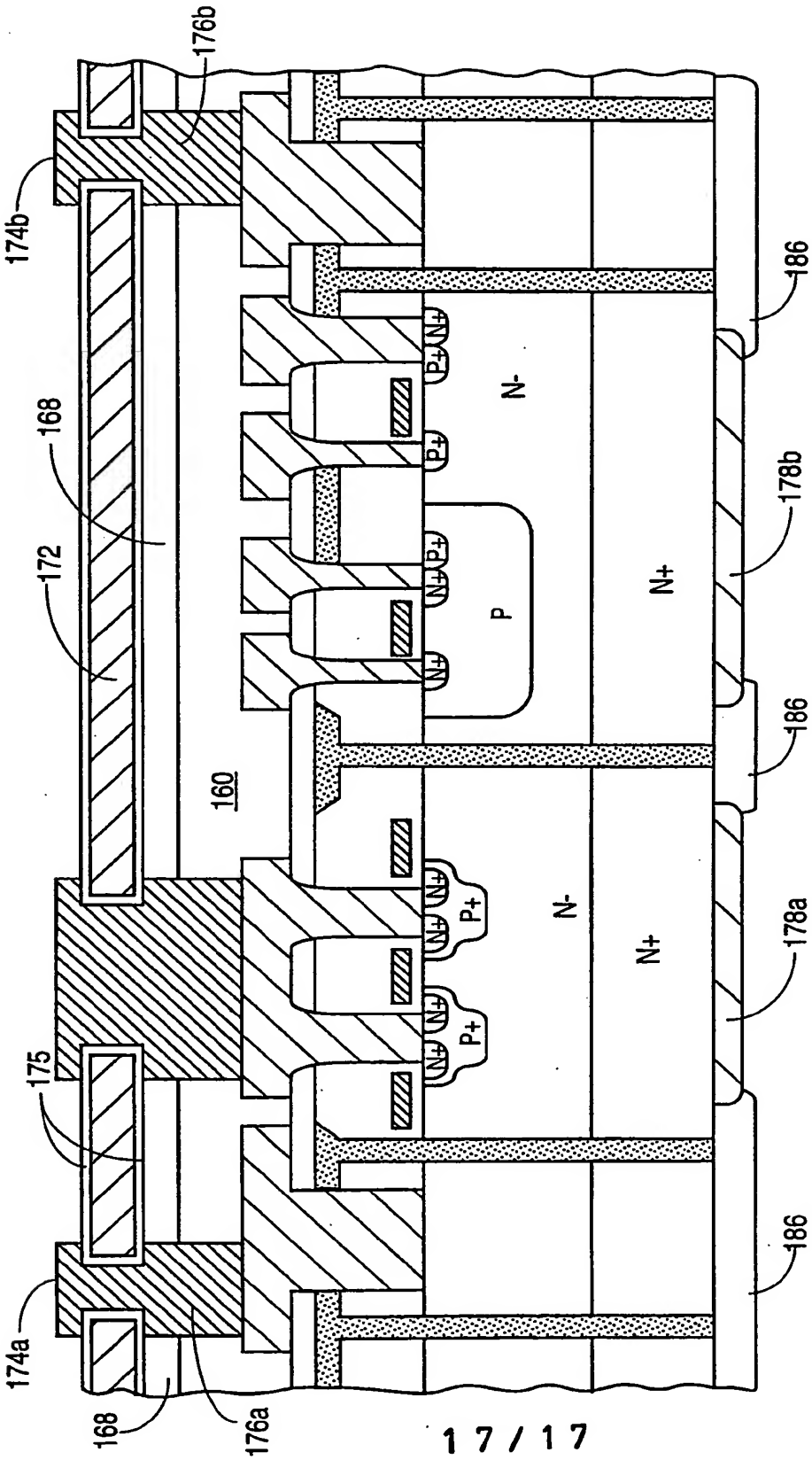


Fig. 16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P+
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N+

Fig. 17

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/05217

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :H01L 23/48, 21/76
US CL :257/631,686,706,724; 437/62,63
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/631,686,706,724; 437/62,63

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

USAPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y, E	US,A 5,426,072 (FINNILA) 20 JUNE 1995, SEE FIGURE 6.	3,5,6, 11,14,15
Y	US,A 5,272,104 (SCHRANTZ ET AL.) 21 DECEMBER 1993, SEE FIGURE 1F.	1-16
Y	US,A 5,229,643 (OHTA ET AL.) 20 JULY 1993, SEE FIGURE 6,30,31.	1-16
Y	US,A 5,170,930 (DOLBEAR ET AL.) 15 DECEMBER 1992, SEE FIGURE 4.	8,13
Y	US,A 5,091,331 (DELGADO ET AL.) 25 FEBRUARY 1992, SEE FIGURE 1E,6,7.	1-16
Y	4,972,250 (OMORI ET AL.) 20 NOVEMBER 1990, SEE WHOLE DOCUMENT	1-16

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search
07 JULY 1995

Date of mailing of the international search report
19 JUL 1995

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